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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,161	PAX, GEORGE E.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 3/10/04. Currently claims 1-63 are pending.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

Rejections under this section have been withdrawn.

Claim Rejections - 35 USC § 102

Claims 1-4, 15-29, and 46-57 stand rejected under 35 U.S.C. 102(e) as being anticipated by Doyle (US6229727).

Regarding claim 1, Doyle discloses a CPU and first and second banks (e.g., col. 2, lines 46-49), with a system bus coupling to the system bus connectors, placing information on the system bus mapped to a first pattern corresponding with said pin assignments of the first memory bank when accessing the first memory bank, and to a second pattern when accessing the second memory bank (e.g., col. 2, lines 54-62).

Regarding claim 2, Doyle also discloses a basic input output system program and a processor, said processor executing said basic input output system program,

wherein said processor places said information on said system bus, said information arranged by said basic input output system in said first pattern when accessing said first memory bank, and in said second pattern when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 3, Doyle also discloses an operating system loaded into said memory device and executed by said processor, said operating system arranged to communicate information to said basic input output system (e.g., col.2, lines 49-53).

Regarding claim 4, Doyle also discloses a plurality of memory modules (e.g., col.3, lines 32-34), and said computer system further comprises a memory controller, said address bus coupling said central processing unit to said memory controller, and said memory controller to each of said plurality of memory modules (e.g., Figure 1, "16", "50").

Regarding claim 15, Doyle also discloses processor and a basic input output system program; a memory module, said memory module comprising a first memory bank, a second memory bank, and a plurality of system bus connectors and a system bus coupling said central processing unit to said plurality of system bus connectors of said memory module (e.g., col. 2, lines 46-49), wherein said central processing unit places information on said system bus in a bit pattern, said bit pattern arranged by said basic input output system to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said bit pattern arranged to a second pattern corresponding with said pin assignments of said second

memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 16, Doyle also discloses a central processing unit having a processor and a basic input output system program; a memory module, said memory module comprising a first memory bank, a second memory bank, and a plurality of system bus connectors, said first and second memory banks each having a plurality of system pin assignments, each of said plurality of system bus connectors connecting to an associated one of said plurality of system pin assignments of said first memory bank, and to an associated one of said plurality of system pin assignments of said second memory bank, wherein at least one of said plurality of system bus connectors connects to non identical system pin assignments of said first and second memory banks (e.g., col. 2, lines 54-62), an operating system run by said processor (e.g., col.2, lines 49-53); and, a system bus coupling said central processing unit to said plurality of system bus connectors of said memory module, wherein said operating system requests information from said processor, and said processor places said information on said system bus mapped by said basic input output system to a first pattern corresponding with said system pin assignments of said first memory bank when accessing said first memory bank, and mapped to a second pattern corresponding with said address pin assignments of said second memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 17, Doyle also discloses central processing unit; a memory module, said memory module comprising: an address bus connector; a first memory

bank, said first memory bank comprising a plurality of address pin assignments coupled to said address bus connector in a first pattern; and, a second memory bank, said second memory bank comprising a plurality of address pin assignments coupled to said address bus connector in a second pattern, wherein said first and second patterns are not identical such that an address at said address bus connector corresponds to a first address read by said first memory bank, and a second address different from said first address read by said second memory bank (e.g., col. 2, lines 54-62); and, an address bus coupling said central processing unit to said address bus connector of said memory module, wherein said central processing unit places an address on said address bus mapped to correspond with said first pattern when accessing said first memory bank, and mapped to correspond with said second pattern when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 18, Doyle also discloses a central processing unit; a system bus coupled to said central processing unit, said system bus comprising a plurality of system bus lines, each of said plurality of system bus lines corresponding to a unique system bus assignment; and, a memory device comprising: a system bus connector coupled to said system bus, said system bus connector comprising a plurality of bus line connectors, each of said plurality of bus line connectors arranged to correspond with a respective one of said system bus lines; a first memory bank comprising a plurality of pins, each said pin corresponding to a unique pin assignment, each of said address pin assignments connected to an associated one of said plurality of bus line connectors such that said pin assignments of said first memory bank are identical to said system

bus assignments; and, a second memory bank comprising a plurality of pin assignments, each of said pin assignments connected to an associated one of said plurality of bus line connectors such that said pin assignments of said second memory bank are not identical to said system bus assignments (e.g., col. 2, lines 54-62), wherein said central processing unit communicates with said memory device by placing information on said system bus, and reading information from said system bus, said information comprising a plurality of bits, each bit associated with one system bus line, and wherein said central processing unit is configured to encode information placed on said system bus to a coded pattern when interfacing with said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 19, Doyle also discloses the coded pattern is defined by rearranging said bits defining said information to correspond to said pin assignments of said second memory bank (e.g., col. 6, lines 30-34).

Regarding claim 20, Doyle also discloses a central processing unit, said central processing unit comprising a processor and a basic input output system program; a memory module, said memory module comprising a first memory bank, a second memory bank, and a plurality of system bus connectors, said first and second memory banks each having a plurality of pin assignments, one pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks (e.g., col.2, lines 54-62), a system bus comprising a plurality of physical bus lines, each of said physical

bus lines coupling said central processing unit to a respective one of said plurality of system bus connectors of said memory module, said system bus arranged to transfer information between said memory module and said central processing unit, said information comprising a plurality of logical bits, one logical bit per physical bus line (e.g., Figure 1), wherein said basic input output system is configured to arrange said information in a first pattern by ordering said plurality of logical bits to bit positions that correspond to said pin assignments of said first memory bank, and said basic input output system is configured to arrange said information in a second pattern by ordering said plurality of logical address bits to bit positions that correspond to said address assignments of said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 21, Doyle also discloses an assignment of at least one logical bit does not correspond with a physical bit assignment of a corresponding physical bus line, but said assignment of said at least one logical bit does correspond with an associated pin assignment to which said at least one logical bit is coupled (e.g., col. 2, lines 54-62).

Regarding claim 22, Doyle also discloses a central processing unit comprising a plurality of system bus connectors, each of said system bus contacts corresponding to a unique bus assignment (e.g., col. 2, lines 54-62).; a system bus comprising a plurality of system bus lines; and, a remap multiplexer switchable from a first state wherein each of said system bus lines are coupled to a corresponding one of said system bus

connectors, to a second state wherein at least two of said bus lines are swapped so as to couple to different ones of said system bus connectors (e.g., col. 6, lines 30-34).

Regarding claim 23, Doyle also discloses wherein said remap multiplexer comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second inputs, an output and a control input (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1), wherein a first one of said system bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said system bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers configured to switch between a first state where said first one of said system bus lines appears at said output of said first multiplexer and said second one of said system bus lines appears at said output of said second multiplexer, and a second state where said second one of said system bus lines appears at said output of said first multiplexer and said first one of said system bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs (col.6, lines 30-34).

Regarding claim 24, Doyle also discloses a memory module coupled to said system bus, said memory module comprising a first memory bank, a second memory bank, and a plurality of system bus connectors, said first and second memory banks each having a plurality of pin assignments, one pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-

identical pin assignments of said first and second memory banks, and each of said plurality of system bus connectors coupling to a corresponding one of said system bus lines (e.g., col. 2, lines 54-62) and, a memory controller coupled to said system bus, said memory controller connected to said control input of each of said first and second multiplexers, wherein said memory controller is configured to toggle said first and second multiplexers in said first state when said central processing unit communicates with said first memory bank, and said memory controller is configured to switch said first and second multiplexers to said second state when said central processing unit communicates with said second memory bank (e.g., col. 6, lines 30-34).

Regarding claim 25, Doyle also discloses wherein said remap multiplexer is coupled to said system bus between said central processing unit and said memory controller (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 2, "20, CAS0").

Regarding claim 26, Doyle also discloses wherein said remap multiplexer is coupled to said system bus between said memory controller and said memory device (e.g., Figure 1).

Regarding claim 27, Doyle also discloses wherein said remap multiplexer is integral with said memory controller (e.g., Figure 1).

Regarding claim 28, wherein said memory controller comprises a buffered system bus driver between said remap multiplexer and said memory device (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 2, "20, CAS0").

Regarding claim 29, Doyle also discloses wherein said memory controller comprises a buffered system bus register, wherein said remap multiplexer is coupled to

said system bus between said buffered system bus register and said memory device (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 2, "20, CAS0").

Regarding claim 46. Doyle discloses a processor; a memory controller; at least one memory module; an address bus coupling said processor to said at least one memory module through said memory controller, said address bus comprising a plurality of address lines (e.g., col. 2, lines 54-62); a command bus coupling said processor to said at least one memory module through said memory controller (e.g., col.6, lines 30-34), said command bus comprising a plurality of command lines; an address remap multiplexer coupled to said address bus, wherein said memory controller is arranged to selectively switch said address remap multiplexer from a first state wherein at least two of said address lines are arranged in a first bit position, to a second state wherein said at least two address lines are remapped to different bit positions; and, a command remap multiplexer coupled to said command bus, wherein said memory controller is arranged to selectively switch said command remap multiplexer from a first state wherein at least two of said command lines are arranged in a first bit position, to a second state wherein said at least two command lines are remapped to different bit positions (e.g., col.6, lines 30-34).

Regarding claim 47, Doyle also discloses wherein said remap multiplexer is switched between said first and second states by a bank select control (e.g., col.6, lines 30-34).

Regarding claim 48, Doyle also discloses a circuit package; a first multiplexer having a first input, a second input, a control signal input, and an output; a second

multiplexer having a first input, a second input, a control signal input, and an output; a first pin extending from said circuit package and coupled to said first input of said first multiplexer and said second input of said second multiplexer; a second pin extending from said circuit package and coupled to said second input of said first multiplexer and said first input of said second multiplexer; a first pin assignment coupled to said output of said first multiplexer; a second pin assignment coupled to said output of said second multiplexer; and, a circuit coupled to said first and second pin assignments, wherein said first and second multiplexers are switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output (e.g., col.6, lines 30-34).

Regarding claim 49, Doyle also discloses first and second pins are arranged in a bilaterally symmetrical arrangement (e.g., Figure 3).

Regarding claim 50, Doyle also discloses a further comprising a third pin extending from said circuit package and coupled to said control signal input of said first and second multiplexers (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 2, "20, CAS0").

Regarding claim 51, Doyle also discloses wherein said control signal input of said first and second multiplexers are coupled to internal logic, said internal logic arranged to switch said first and second multiplexers between said first and second states (e.g., col.6, lines 30-34).

Regarding claim 52, Doyle also discloses a mode register (e.g., col. 7, lines 13-20).

Regarding claim 53, Doyle also discloses a circuit package; a circuit contained within said circuit package; a plurality of pins extending from said circuit package (e.g., Figure 2), a remap multiplexer contained within said circuit package, said reroute multiplexer circuit comprising: a first multiplexer having a first input, a second input, a control signal input, and an output, said first input coupling to a first one of said pins and said second input coupled to a second one of said pins; a second multiplexer having a first input, a second input, a control signal input, and an output, said first input coupled to said second one of said pins and said second input coupled to said first one of said pins; a first pin assignment coupling said output of said first multiplexer to said circuit; and, a second pin assignment coupling said output of said second multiplexer to said circuit, wherein said remap multiplexer is switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output (e.g., Figure 2, "MUX", "DRAM_MUX_L").

Regarding claim 54, Doyle also discloses wherein said control signal input of said first and second multiplexers are each coupled to a third one of said plurality of pins on said memory device (e.g., Figure 2, "MUX", "DRAM_MUX_L").

Regarding claim 55, Doyle also discloses wherein said control signal inputs of said first and second multiplexers are coupled to internal logic, said internal logic

arranged to switch said remap multiplexer between said first and second states (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 56, Doyle also discloses a mode register (e.g., col. 7, lines 13-20).

Regarding claim 57, Doyle also discloses a circuit package; a plurality of pins extending from said circuit package; an memory circuit internal to said circuit package; a plurality of pin assignments coupled to said memory circuit (e.g., Figure 2, "20"); and, a remap multiplexer contained within said circuit package, said remap multiplexer coupling said plurality of pins to said plurality of internal pin assignments, and having a control input, wherein said control signal is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Thus are claims 1-4, 15-29, and 46-57 rejected.

Claim Rejections - 35 USC § 103

Claims 5, 30, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle in view of well-known features of circuit packages, as further evidenced by Miller (US 5808897).

Regarding claim 5, Doyle also discloses a substrate; at least one memory chip mounted on said substrate defining said first memory bank, each said at least one memory chip having a plurality of pins, one pin associated with a respective one of said plurality of pin assignments; at least one memory chip mounted on said substrate defining said second memory bank, each said memory chip having a plurality of pins, one pin associated with a respective one of said plurality of pin assignments (e.g., Figure 1, "20", "22"); and, a plurality of circuit traces, each circuit trace coupling one pin assignment from each said first and second memory banks to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks (e.g., col. 2, lines 54-62). Doyle does not expressly mention pads; however Examiner takes Official Notice that these are well known features of memory circuit packages such as that of Doyle. This is further evidenced by Miller. Miller discloses that a circuit package has a plurality of pads mounted along one edge of said substrate (e.g., col. 3, line 7). It would be obvious to one of ordinary skill in the art to combine these features because it is commonly known that these features are a well-known aspect of a circuit package. Therefore it would be obvious to combine Doyle with well-known features of circuit packages, as evidenced by Miller, at the time the invention was made, to obtain the claimed invention.

Regarding claim 30, Doyle also discloses a substrate; at least one memory chip mounted on said substrate defining said first memory bank, each said memory chip having a plurality of pins, one pin associated with a respective one of said plurality of pin

assignments; at least one memory chip mounted on said substrate defining said second memory bank, each said memory chip having a plurality of pins, one pin associated with a respective one of said plurality of pin assignments; and, a plurality of circuit traces, each circuit trace coupling one pin assignment from each said first and second memory banks to an associated one of said plurality of system bus connectors (e.g., Figure 1, "20", "22"), wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks (e.g., col. 2, lines 54-62). Doyle does not expressly mention pads; however Examiner takes Official Notice that these are well known features of memory circuit packages such as that of Doyle. This is further evidenced by Miller. Miller discloses that a circuit package has a plurality of pads mounted along one edge of said substrate (e.g., col. 3, line 7). It would be obvious to one of ordinary skill in the art to combine these features because it is commonly known that these features are a well-known aspect of a circuit package. Therefore it would be obvious to combine Doyle with well-known features of circuit packages, as evidenced by Miller, at the time the invention was made, to obtain the claimed invention.

Regarding claim 58, Doyle also discloses a substrate; at least one memory chip mounted on said substrate defining a first memory bank, each said at least one memory chip comprising: a circuit package; a plurality of pins extending from said circuit package; an memory circuit internal to said circuit package; a plurality of pin assignments coupled to said memory circuit (Figure 2, "20"); and, a remap multiplexer contained within said circuit package, said remap multiplexer coupling said plurality of

pins to said plurality of internal pin assignments, and having a control input, wherein said control signal is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments (e.g., col.6, lines 30-42, "DRAM_MUX_L"); at least one memory chip mounted on said substrate defining a second memory bank, each of said at least one memory chip comprising: a circuit package; a plurality of pins extending from said circuit package; an memory circuit internal to said circuit package; a plurality of pin assignments coupled to said memory circuit; and, a remap multiplexer contained within said circuit package, said remap multiplexer coupling said plurality of pins to said plurality of internal pin assignments, and having a control input, wherein said control signal input is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments (e.g., col.6, lines 30-42, "DRAM_MUX_L"). Doyle also discloses a circuit package, but does not expressly mention the details of pads and traces; however Examiner takes Official Notice that this are well known features of memory circuit packages such as that of Doyle. This is further evidenced by Miller. Miller discloses that a circuit package has a plurality of pads mounted along one edge of said substrate (e.g., col. 3, line 7); and, a plurality of circuit traces (e.g., col. 3, line 13). It would be obvious to one of ordinary skill in the art to combine these features of a circuit package because it is commonly known that these features are a well-known aspect of a circuit

package. Therefore it would be obvious to combine Doyle with well-known features of circuit packages, as evidenced by Miller, at the time the invention was made, to obtain the claimed invention.

Claims 6-14, 31-45, and 59-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle in view of Miller.

Regarding claim 6, Doyle does not expressly mention the disposition of the memory modules; however this feature is well known in the art as evidenced by Miller. Miller discloses memory modules on first and second major surfaces (e.g., col. 1, lines 42-50). It would be obvious to combine Miller with Doyle because the Miller teaches the advantage of mounting memory modules on both sides of a substrate, in order to increase packing density, such as in the instance of the memory modules of Doyle. Therefore it would be obvious to one of ordinary skill in the art to combine Miller with Doyle, as applied in claim 5 above, at the time the invention was made.

Regarding claim 7, Doyle also discloses identical number and configuration of memory chips (e.g., col. 2, lines 63-67). Miller also discloses the physical detail of mounting the memory chips in register (e.g., col. 1, lines 61-64).

Regarding claim 8, Miller also discloses a plurality of vias, each of said vias adjacent to, and coupling a select one of said plurality of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface (e.g., col. 1, lines 39-41).

Regarding claim 9, Miller also discloses wherein: each said memory chip comprises a plurality of address pins arranged bilaterally symmetrical; each of said plurality of address pins is associated with a respective one of a plurality of internal address pin assignments; and, said plurality of vias positioned on said substrate such that each via is adjacent to, and couples a select one of said plurality of address pins having a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins having a second pin assignment and the plurality of address bus connectors (e.g., col. 1, lines 39-41, Figure 1A, 1B). Doyle discloses where the second pin assignment is different from the first pin assignment (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 10, Doyle also discloses an address bus coupled between said central processing unit and said address bus connectors, wherein said central processing unit places an address on said address bus mapped to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said address mapped to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 11, Doyle also discloses a plurality of address bits, said first pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin assignments of said address pins of said first memory bank, and said second pattern comprises arranging said plurality of address bits in a sequence

that aligns with the corresponding pin assignments of said address pins of said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 12, Miller also discloses each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical; each of said plurality of command pins associated with a respective one of said plurality of pin assignments; and, said plurality of vias are arranged on said substrate such that each via is adjacent to, and couples a select one of said plurality of command pins having a first pin assignment and positioned on said first major surface, to a select one of said plurality of command pins having a second pin assignment (e.g., col. 1, lines 39-41, "address"). Doyle discloses the second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality command bus connectors (e.g., col. 2, lines 54-62).

Regarding claim 13, Doyle also discloses wherein said system bus further comprises a command bus coupled between said central processing unit and said command bus connectors, wherein said central processing unit places a command on said command bus mapped to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said command mapped to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 14, Doyle also discloses wherein said command comprises a plurality of command bits, said first pattern comprises arranging said plurality of

command bits in a sequence that aligns with the corresponding pin assignments of said command pins of said first memory bank, and said second pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins defining said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 31, Doyle does not expressly mention the disposition of the memory modules; however this feature is well known in the art as evidenced by Miller. Miller discloses memory modules on first and second major surfaces (e.g., col. 1, lines 42-50). It would be obvious to combine Miller with Doyle because the Miller teaches the advantage of mounting memory modules on both sides of a substrate, in order to increase packing density, such as in the instance of the memory modules of Doyle. Therefore it would be obvious to one of ordinary skill in the art to combine Miller with Doyle at the time the invention was made.

Regarding claim 32, Doyle also discloses identical number and configuration of memory chips (e.g., col. 2, lines 63-67). Miller also discloses the physical detail of mounting the memory chips in register (e.g., col. 1, lines 61-64).

Regarding claim 33, Miller also discloses a plurality of vias, each of said vias adjacent to, and coupling a select one of said plurality of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface (e.g., col. 1, lines 39-41).

Regarding claim 34, Miller also discloses wherein: each said memory chip comprises a plurality of address pins arranged bilaterally symmetrical; each of said

plurality of address pins is associated with a respective one of a plurality of pin assignments; and, said plurality of vias positioned on said substrate such that each via is adjacent to, and couples a select one of said plurality of address pins having a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins having a second pin assignment and the plurality of address pins (e.g., col. 1, lines 39-41, Figure 1A, 1B). Doyle discloses where the second pin assignment is different from the first pin assignment (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 35, Doyle also discloses wherein said system bus further comprises an address bus coupling said central processing unit, said memory controller, said remap multiplexer and said address bus connectors, wherein said central processing unit places an address on said address bus and said remap multiplexer maps said address to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said remap multiplexer maps said address to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 36, Doyle also discloses wherein said address comprises a plurality of address bits, said first pattern comprises arranging said plurality of address to bits in a sequence that aligns with the corresponding pin assignments of said address pins of said first memory bank, and said second pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin

assignments of said address pins defining said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 37, Doyle also discloses wherein the remap multiplexer comprises a multiplexing circuit for each pair of address pins, each of said multiplexing circuits arranged to switchably swap address lines associated with said respective address pins (e.g., col.6, lines 30-42, "DRAM_MUX_L"). Miller discloses the bilaterally symmetrical address pins (e.g., col. 1, lines 45-50).

Regarding claim 38, Doyle also discloses each multiplexing circuit comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second input, an output and a control input, wherein a first one of said address bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said address bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers switching between a non-switched state where said first one of said address bus lines appears at said output of said first multiplexer and said second one of said address bus lines appears at said output of said second multiplexer, and a switched state where said second one of said address bus lines appears at said output of said first multiplexer and said first one of said address bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 39, Doyle also discloses wherein said memory controller has a control signal coupled to each said control inputs of said first and second multiplexers of

each said multiplexing circuits, said memory controller arranged to switch said control inputs such that all said first and second multiplexers are in said non-switched state or all said first and second multiplexers are in said switched state (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 40, Miller also discloses wherein: said plurality of system bus connectors further comprise a plurality of command bus connectors; each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical; each of said plurality of command pins associated with a respective one of said plurality of pin assignments and, said plurality of vias arranged on said substrate such that each via is adjacent to, and coupling a select one of said plurality of command pins (e.g., col. 1, lines 39-41, "address"). Doyle also discloses having a first pin assignment and positioned on a first major surface, to a select one of said plurality of command pins having a second pin assignment different from said first pin assignment, and located on a second major surface, to a respective one of said plurality of command bus connectors (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 41, Doyle also discloses wherein said system bus further comprises a command bus coupling said central processing unit, said memory controller, said remap multiplexer and said command bus connectors, wherein said central processing unit places a command on said command bus and said remap multiplexer maps said command to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said remap multiplexer maps said command to a second pattern corresponding with

said pin assignments of said second memory bank when accessing said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 42, Doyle also discloses wherein said command comprises a plurality of command bits, said first pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins of said first memory bank, and said second pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins defining said second memory bank (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 43, Doyle also discloses wherein said remap multiplexer comprises a multiplexing circuit for each pair of bilaterally symmetrical command pins, each of said multiplexing circuits arranged to switchably swap command lines associated with said respective symmetrical command pins (e.g., Figure 3).

Regarding claim 44, Doyle also discloses wherein each said multiplexing circuit comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second input, an output and a control input, wherein a first one of said command bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said command bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers switching between a non-switched state where said first one of said command bus lines appears at said output of said first multiplexer and said second one of said command bus lines appears at said

output of said second multiplexer, and a switched state where said second one of said command bus lines appears at said output of said first multiplexer and said first one of said command bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 45, Doyle also discloses wherein said memory controller has a control signal coupled to each said control inputs of said first and second multiplexers of each said multiplexing circuits, said memory controller arranged to switch said control inputs such that all said first and second multiplexers are in said non-switched state or all said first and second multiplexers are in said switched state (e.g., col.6, lines 30-42, "DRAM_MUX_L"; Figure 1).

Regarding claim 59, Doyle does not expressly mention the disposition of the memory modules; however this feature is well known in the art as evidenced by Miller. Miller discloses memory modules on first and second major surfaces (e.g., col. 1, lines 42-50). It would be obvious to combine Miller with Doyle because the Miller teaches the advantage of mounting memory modules on both sides of a substrate, in order to increase packing density, such as in the instance of the memory modules of Doyle. Therefore it would be obvious to one of ordinary skill in the art to combine Miller with Doyle at the time the invention was made.

Regarding claim 60, Doyle also discloses identical number and configuration of memory chips (e.g., col. 2, lines 63-67). Miller also discloses the physical detail of mounting the memory chips in register (e.g., col. 1, lines 61-64).

Regarding claim 61, Miller also discloses a plurality of vias, each of said vias adjacent to, and coupling a select one of said plurality of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface (e.g., col. 1, lines 39-41).

Regarding claim 62, Miller also discloses wherein: each said memory chip comprises a plurality of address pins arranged bilaterally symmetrical; each of said plurality of address pins is associated with a respective one of a plurality of internal address pin assignments; and, said plurality of vias positioned on said substrate such that each via is adjacent to, and couples a select one of said plurality of address pins having a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins having a second pin assignment and the plurality of traces (e.g., col. 1, lines 39-41, Figure 1A, 1B). Doyle discloses where the second pin assignment is different from the first pin assignment wherein said remap multiplexers in said first bank are switched to said first state, and said remap multiplexers in said second bank are switched to said second state (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Regarding claim 63, Miller also discloses each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical each of said plurality of command pins associated with a respective one of a plurality of internal control pin assignments; and, said plurality of vias are arranged on said substrate such that each via is adjacent to, and couples a select one of said plurality of command pins having a first pin assignment and positioned on said first major surface, to a select one of said plurality of

command pins (e.g., col. 1, lines 39-41, "address"). Doyle discloses the second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of circuit traces, and wherein said remap multiplexers in said first bank are switched to said first state, and said remap multiplexers in said second bank are switched to said second state (e.g., col.6, lines 30-42, "DRAM_MUX_L").

Response to Arguments

Applicant's arguments filed 3/10/04 have been fully considered but they are not persuasive.

Regarding independent claims 1, 15-18, 20, 22, and 46, Applicant argues that recitation of memory chips as "substantially identical" serves to distinguish over Doyle, arguing that Doyle "supports 'different sizes and configurations of random access memory in a single DIMM socket'" (p. 27); however Examiner deems memory chips of Doyle to be substantially identical. Doyle teaches a "system for accommodating a plurality of memory devices in a single DIMM socket" (col. 3, lines 32-33), which is reasonably interpreted to mean substantially identical memory banks. The different memory sizes result in "non-identical pin assignments", as also recited in the claims. Although the insubstantial differences of the claimed invention, which result in "non-identical pin assignments" might be interpreted to mean something that distinguishes over Doyle's features, this distinction finds no weight in the claims.

Applicant argues that claims 2-4, 19, 21, 23-29, and 47, "recite further limitations not shown or suggested by the prior art" (p. 27); however, all limitations are deemed disclosed by Doyle and supported by citations maintained supra.

Thus the rejection of 1-4, 15-29, and 46-47 is maintained.

Regarding claims 48, 53, and 57, Applicant argues that Doyle fails "to provide for multiplexers contained within an integrated circuit memory chip"; however the recitation merely supports a "multiplexer contained with said circuit package". Doyle teaches a multiplexer that renders a "memory device that is 'transparent' to the microprocessor" (col. 2, lines 61-62), and "for the appropriate connections to the desired memory address lines to be already present" (col. 2, lines 51-53). Broadly interpreted, this comprises the "circuit package" of the claimed invention. Any particular physical configuration of the invention lacks adequate support in the claims to distinguish.

Regarding claims 5, 30, and 58, rejected under 103(a), Applicant argues that Doyle "fails to disclose identical memory chips as well as remap multiplexers contained with the circuit package of the memory chip itself", both of which have been dealt with supra.

Applicant further argues that Miller fails to remedy the deficiencies of Doyle; arguing that Miller fails to disclose "identical memory chips" nor "remap multiplexers"; however these are features that rely on Doyle, as treated supra (i.e., as *substantially* identical memory chips, as claimed), and not on Miller.

Applicant argues that dependent claims 6-14, 31-45, and 59-63 include additional limitations, which distinguish them from the prior art; however no specific examples are

argued. Hopefully the prior art citations above make clear the interpretation relied upon in the rejection.

Thus rejections of 5-14, 30-45, 58-63 are maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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